

2.5V Drive Pch+Pch MOS FET

QS6J3

●Structure

Silicon P-channel MOS FET

●Features

- 1) Two Pch MOS FET transistors in a single TSMT6 package.
- 2) Low on-state resistance with a fast switching.
- 3) Low voltage drive (2.5V).

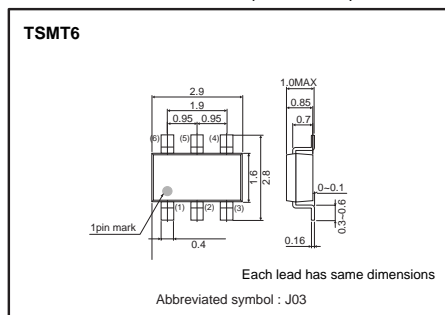
●Applications

Switching

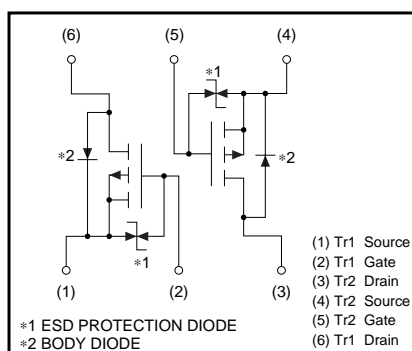
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS6J3		○

●External dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for Tr1 and Tr2 >

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DSS}	-20	V	
Gate-source voltage	V_{GSS}	±12	V	
Drain current	Continuous	I_D	±1.5	A
	Pulsed	I_{DP} *1	±6.0	A
Source current (Body diode)	Continuous	I_S *1	-0.75	A
	Pulsed	I_{SP}	-6.0	A
Total power dissipation	P_D *2	1.25	W / TOTAL	
		0.9	W / ELEMENT	
Channel temperature	T_{ch}	150	°C	
Range of Storage temperature	T_{stg}	-55 to +150	°C	

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$ *2 Mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th}(ch-a)$ *	100	°C / W / TOTAL
		139	°C / W / ELEMENT

* Mounted on a ceramic board

Transistors

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2. MOS FET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	±10	μA	V _{GS} =±12V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	-20	–	–	V	I _D = -1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	-1	μA	V _{DS} = -20V, V _{GS} =0V
Gate threshold voltage	V _{GS (th)}	-0.7	–	-2.0	V	V _{DS} = -10V, I _D = -1mA
Static drain-source on-state resistance	R _{DS (on)} *	–	155	215	mΩ	I _D = -1.5A, V _{GS} = -4.5V
		–	170	235	mΩ	I _D = -1.5A, V _{GS} = -4V
		–	310	430	mΩ	I _D = -0.75A, V _{GS} = -2.5V
Forward transfer admittance	Y _{fs} *	1.0	–	–	S	V _{DS} = -10V, I _D = -0.75A
Input capacitance	C _{iss}	–	270	–	pF	V _{DS} = -10V
Output capacitance	C _{oss}	–	40	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	–	35	–	pF	f=1MHz
Turn-on delay time	t _{d (on)} *	–	10	–	ns	I _D = -0.75A
Rise time	t _r *	–	12	–	ns	V _{DD} ≐ -15V V _{GS} = -4.5V
Turn-off delay time	t _{d (off)} *	–	45	–	ns	R _L =20Ω
Fall time	t _f *	–	20	–	ns	R _G =10Ω
Total gate charge	Q _g *	–	3.0	–	nC	V _{DD} ≐ -15V R _L =10Ω
Gate-source charge	Q _{gs} *	–	0.8	–	nC	V _{GS} = -4.5V R _G =10Ω
Gate-drain charge	Q _{gd} *	–	0.85	–	nC	I _D = -1.5A

*Pulsed

<Body diode (Source-drain)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD}	–	–	-1.2	V	I _S = -0.75A, V _{GS} =0V

Transistors

●Electrical characteristic curves

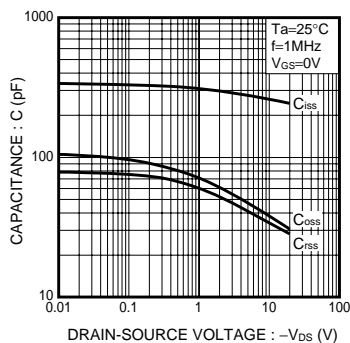


Fig.1 Typical Capacitance vs. Drain-Source Voltage

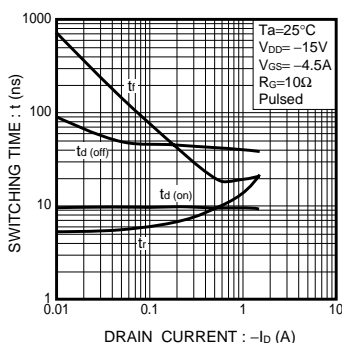


Fig.2 Switching Characteristics

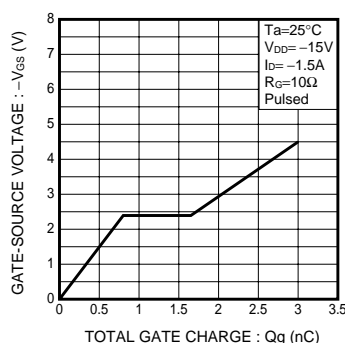


Fig.3 Dynamic Input Characteristics

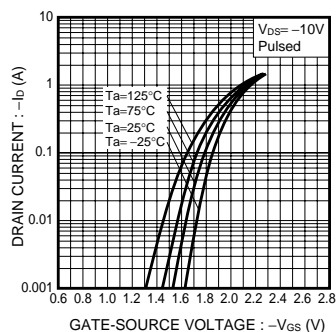


Fig.4 Typical Transfer Characteristics

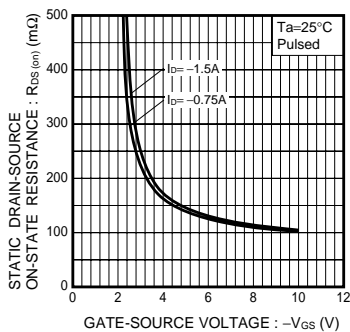


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

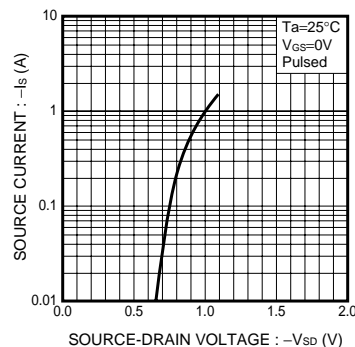


Fig.6 Source Current vs. Source-Drain Voltage

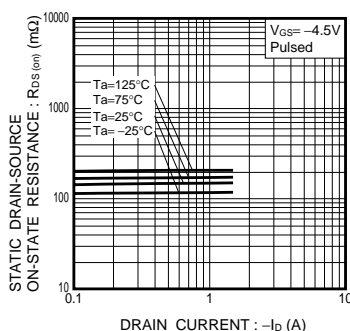


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

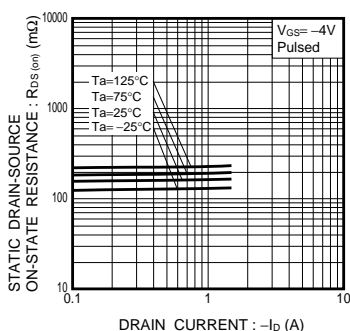


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

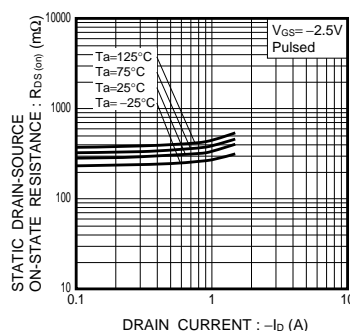


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Transistors

●Measurement circuits

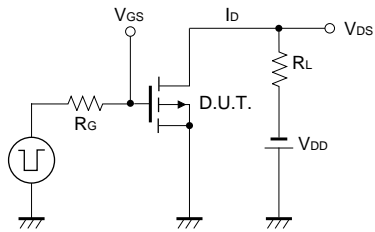


Fig.10 Switching Time Measurement Circuit

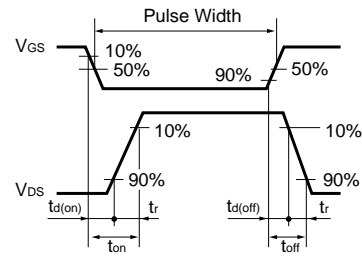


Fig.11 Switching Waveforms

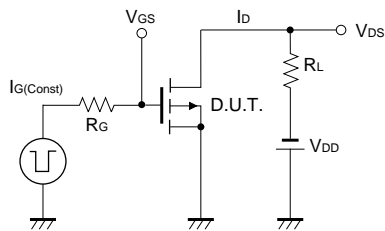


Fig.12 Gate Charge Measurement Circuit

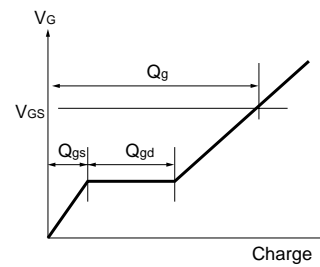


Fig.13 Gate Charge Waveform

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